SystemC Components Library
SCC

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What is SCC

- SCC is an open-source productivity library
- As such it provides common functions, components and modules often needed in SystemC based models
- In-use at customers of MINRES
- Relies on C++11
- SystemC version >= 2.3.1
- Utilizes SystemC CCI

SCC Elements

- Common build system
- PySysC binding
- Modular structure

Module	Content
common	SystemC independent functions and components
sysc	Common SystemC and TLM related functionalities and components
components	VP components, mainly for LT modeling
bus_interfaces	TLM2.0 protocol abstractions and sockets as well as AT drivers, targets, and pin-level adapter

Build System

- CMake based build system
- Supports conan.io for 3rd party packages (even SystemC and CCI are available this way)
- Supports Windows and Linux (various compiler versions)
- Supports OSCI as well as SNPS PA, CDNS Xcelium, and MINRES RAVEN SystemC transparently
- Integrates Verilator, doxygen, clang-format, and clang-tidy

Module common

- Provides non-SystemC utilities
  - Simple C++ logging system
  - Thread safe pool allocator with debugging aids
  - Generic bitfield implementation
  - Pseudo random number generator (PRNG)
  - Watchdog
  - Multi-thread synchronization elements
  - Range based lookup-table

Module sysc: SystemC related

- Enhanced high-performance reporting system allowing instance base log configuration
- Configuration module to read JSON input and apply values to sc_attributes as well as CCI parameters
- Tracer module to automatically trace signals, ports, and variables
- Semaphore with guaranteed order of granting
- Reproducible PRNG (based on SystemC processes)

Module sysc: TLM2.0 related

- TLM2.0 pool allocator with memory leak debugging aids
- Generic payload shared pointer to ease memory handling
- Transaction recording of the generic protocol incl. extensions
- Socket mixins to add capabilities to standard TLM sockets (e.g. translate B<->NB or transaction tracing)

Module components

- Clock converter (sc_time <-> bool)
- Arbitrary size memory (sparse array implementation)
- LT M-to-N router with configurable address decoding and translation
- Generic TLM2.0 target to handle register file access
- Simple register with bitfield and callback support
  - Allows to generate register fields from SystemRDL and IP-XACT

Module busses

- Protocol definitions
- Socket definitions
- Initiator and target protocol engines
- Transaction recorders
- Bus-functional models aka pin-level adapters

Supported Protocols

- APB
- AHB
- AXI
- ACE
- CHI
- OBI

Not all combinations and conversions are available (yet)

Licensing

- Apache 2.0 license
- SCC comes with 3rd party libs
  - jsoncpp: MIT
  - spdlog: MIT
  - SCV-TR (stripped version of SCV): Apache 2.0
  - Arteris tlm_interface definitions: Apache 2.0